A Unified Yield Model Incorporating Both Defect and Parametric Effects

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***Abstract*— A new approach to modeling yield is presented, which inherently includes both the effects of the conventional defect contributors and the parametric yield loss contributors often treated separately in existing yield models. These parametric yield losses are particularly important during the startup yield-improvement phase of new technology introduction, in many performance-sensitive products such as analog devices and high-speed digital devices, and in analyses of bin-split yields. By assuming a distribution in the size of defects, from point defects up to defects as large as or larger than a wafer, the parametric yield contributors can be viewed as simply rather large, design-dependent defects, which will render IC's unacceptable if any portion of the large defect overlaps the defect-sensitive area of a chip. In this way, the conventional Poisson model, or various extensions of the well-known Murphy model, can be augmented in a straightforward and general way to include parametric yield loss. It is shown that parametric yield losses introduce an additional die size dependence for yield that can help to account for the observed dependence of yield on die area. The model is compared to other models and to experimental yield data to illustrate both its utility in separating yield contributors and its close agreement with experimental yield data.**

I. INTRODUCTION

ACCURATE modeling of integrated circuit yield has been found to be a difficult task. The original yield model of Murphy [1] is widely used, particularly in forms which include some distribution in the mean defect density [2]–[8], but even forms of this model which include empirically determined parameters often fail to fit the experimental data accurately [6]. Furthermore, because of the assumptions incorporated in some models it is often difficult to relate observed yield performance in detail to specific yield loss contributors [8]. Despite these shortcomings, however, such models have been used effectively in yield management [9], and provide a generally accepted description for comparing yield performance [10].

An additional shortcoming of the Murphy model and some yield models derived from it is the inherent assumption that all yield loss, other than that which destroys entire wafers, arises from point defects or from particulate defects which are small compared to the size of the die. While many of the defects and defect types that can cause yield loss fit this description, some yield limiters arise from physical or electrical parameters being out of acceptable range on the die. These parametric problems often affect entire wafers, but Ham [11] has pointed out that such parametric "defects" can also result in variable sized areas of the wafers exhibiting zero yield. He suggested that they can be accounted for by adding a constant yield multiplier called the area usage factor (AUF) to defect-based yield models. A number of authors have subsequently defined an empirical constant Y_0, consistent with this area usage factor concept, to account for both parametric and other similar kinds of large area yield loss on the wafer [6], [9]. It has been added either into the Poisson model or into extensions of the Murphy model as an independent yield loss multiplier to provide better agreement with experimental observations.

One potential problem with such treatments of parametric yield losses is the implied assumption that there is no die size dependence of the loss. While this is expected to be a good assumption when the parametric yield problems impact entire wafers, when examinations of yield wafer maps indicate that they impact only portions of wafers, perhaps over areas that may cover only a few dice [11], [12], such an assumption may be inadequate. In such cases the wafer area impacted by this yield loss will have some die size dependence because of the dice affected around the edges of such regions.

In this paper it is shown that both the conventional small defects and these much larger parametric or area "defects" can inherently be included in most commonly used yield models in a straightforward manner. The resulting yield expression not only provides an analytical expression for the contribution to a constant multiplier Y_0 from the larger defects on wafers, it also includes an additional die-perimeter-dependent yield term which results from the loss of those dice which only partially overlap the large defects. The equations are based only on the defect density distribution as a function of defect size. The model is first described and developed, then compared to previous models, to published data, and to specific experimental data from a commercial silicon integrated circuit factory. Although defect clustering effects can easily be incorporated into the model, it is shown that the model based only on a simple Poisson yield expression can account for much of the observed and published dependence of yield on die area. Similar agreement can be obtained from a number of yield models based on defect clustering, and therefore such agreement by itself does not prove the applicability of the model presented here in explaining any particular set of yield data. However, it does indicate there is an additional and alternative explanation to that of defect clustering for an experimentally-determined dependence of yield on die area. Furthermore the utility of the model in separating yield loss contributors associated with a subset of the total process steps may make it attractive for yield analysis in those cases where it provides a good approximation to observed results.

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II. Variable Defect Size Yield Model

Most yield treatments begin with the assumption that there is a random distribution of point defects characterized by some average defect density D_0, with each defect being statistically independent of all others. Under this assumption the yield Y of an integrated circuit with a critical area A sensitive to such defects is simply the probability of having zero defects within the area A, and is given by the Poisson distribution

$$Y = exp(-AD_0). \tag{1}$$

This equation was found to poorly represent the observed yield as a function of die area in general, and Murphy [1] proposed that the mean defect density might be better viewed as a distribution $f(D)$ which may vary from die to die on each wafer and/or from wafer to wafer to help account for the discrepancy with experiment. Under this assumption it was proposed that (1) be modified to

$$Y = \int f(D) \exp(-AD)\, dD. \tag{2}$$

While Hu [4] has suggested that this equation is not mathematically exact in general, under certain conditions such as when D varies from wafer to wafer it serves as a rather good approximation. A number of authors [1]–[3], [6], [7] have used (2) and several different assumptions about the defect density distribution to derive closed-form solutions, and have found that the resulting yield expressions can provide good agreement with experimental data of yield versus die area. In order to incorporate the contribution of parametric and other large-area yield losses, some authors have further modified (2) with a multiplicative constant [6], [9] as discussed previously to give

$$Y = Y_0 \int f(D) \exp(-AD)\, dD \tag{3}$$

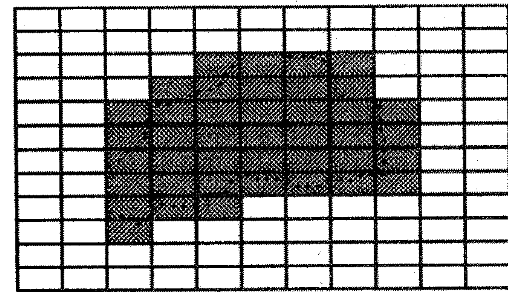
where Y_0 reflects the reduced wafer area which is defect limited in yield, and would include the AUF described, for example, by Ham [11].

Most yield models used today are based on (1), (2), and/or (3). One commonly applied yield expression, derived from (3) assuming the mean defect density is approximated by the gamma distribution function, is referred to as the negative binomial (NB) model [3], [6].

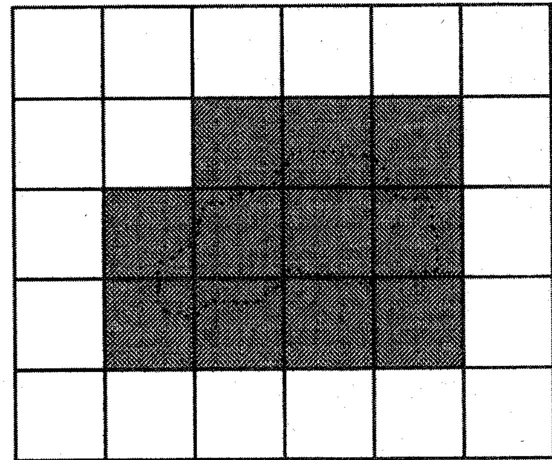
$$Y = Y_0(1 + D_0A/\alpha)^{-\alpha} \tag{4}$$

where D_0 is the mean defect density and α is defined as the clustering parameter. This yield model will be compared later in this paper to the variable defect size model proposed here.

Inherent in (3) and (4) are the assumptions that the parametric yield loss can be adequately addressed by adding an empirical multiplicative constant, and that the only die size dependence of yield comes from small defects through (1) or (2). However, if parametric yield losses can affect only portions of a wafer as described by Ham [11], then it might be expected that a die-size dependence of yield could result from the contribution of dice overlapping the edges of such regions. Fig. 1 demonstrates how a such die size dependence of parametric yield can occur. In the figure an illustrative region shown by the dotted outline represents an area on a wafer that has a parametric problem causing zero yield for any dice that overlap the region. Fig. 1(a) and (b) shows by the shaded areas all dice that will be impacted by this same sized parametric problem for two different die sizes. It can be seen that the wafer area within which dice will fail because of the parametric problem is larger than the dotted region, and covers a somewhat larger total area for the larger die size than for the smaller die size. For this reason an assumption of a die-size-independent area usage factor or Y_0 will fail to accommodate this die-size dependence of the total failure area.



(a)



(b)

Fig. 1. Illustration of the die size dependence of yield loss associated with parametric yield limiters. The dotted outline represents a region of the wafer with unacceptable parameters, and the shaded areas represent the dice lost due to the parametric problem for two different die sizes.

In order to address this aspect of parametric yield loss, it will be assumed here that the defects incorporated in (1) include a distribution of defect size s, where s can vary from zero to a size even comparable to or larger than that of the wafer. If such defects overlap any part of the critical area of a die that is sensitive to that defect, the die is assumed to be bad. Then (1) can be written as

$$Y = \exp\left\{-\int A(s)D(s)\, ds\right\} \tag{5}$$

where $D(s)$ represents the mean density of defects of size s and $A(s)$ is the critical area associated with the die sensitive to a defect of size s.

The concept of A in (5) being dependent on defect size has been previously proposed to address the yield impact of variable-sized particulate defects [9]. In that treatment the defects under consideration were comparable to or smaller than the features on the die, and the critical die area was often found to be smaller than the actual die area for the smaller defects. Furthermore, such a critical area will not only depend on the defect under consideration, it will also depend on the integrated circuit design. However, when the defects become much larger than the features on the die, effectively all such defects will cause a yield loss if the defect is located anywhere within the actual die area because they will invariably overlap some portion of the critical regions. Thus for such larger defect sizes the critical area becomes essentially equal to the actual die area. In what follows this possible critical area dependence on defect size for the smaller defect sizes will be omitted in the interests of simplicity, although it is straightforward to include it later should it be important.

Here, we are particularly interested in defects that are comparable to or larger than the die. In such cases, the critical area must be even larger than the actual die area itself as shown in Fig. 2, because defects located outside the actual die area but with sufficient size to overlap some portion of the die will also result in a yield loss. Such larger defects will often have irregular shapes, so that a general closed-form solution to (5) is not possible. However, the characteristics of (5) for these larger defects can be illustrated by assuming the larger defects are circular in shape with diameter s. In this case the effective area sensitive to such defects includes the die itself and a region around the die within a distance of $s/2$ as shown in Fig. 2. Taking into account this total critical area, (5) becomes

$$\begin{aligned} Y &= \exp\{-\int [LW + (L+W)s + \pi s^2/4] D(s)\,ds\} \\ &= \exp\left\{-LW\int D(s)\,ds - (L+W)\int sD(s)\,ds \right. \\ &\quad \left. - (\pi/4)\int s^2 D(s)\,ds\right\} \\ &= \exp\{-LWD_0 - (L+W)\langle s\rangle D_0 - \langle s^2\rangle D_0\} \end{aligned} \tag{6}$$

where

$$D_0 = \text{mean defect density} = \int D(s)\,ds \tag{7}$$

$$\langle s\rangle = \int sD(s)\,ds/D_0 \tag{8}$$

and

$$\langle s^2\rangle = (\pi/4)\int s^2 D(s)\,ds/D_0. \tag{9}$$

The terms $\langle s\rangle$ and $\langle s^2\rangle$ can be interpreted as weighted means for the defect size and the square of the defect size respectively.

Equation (6) can be written in the form of a product of two exponential terms to illustrate its utility in separating yield loss contributors

$$\begin{aligned} Y = Y_d Y_s &= \exp\{-LWD_0\} \\ &\cdot \exp\{-(L+W)\langle s\rangle D_0 - \langle s^2\rangle D_0\}. \end{aligned} \tag{10}$$

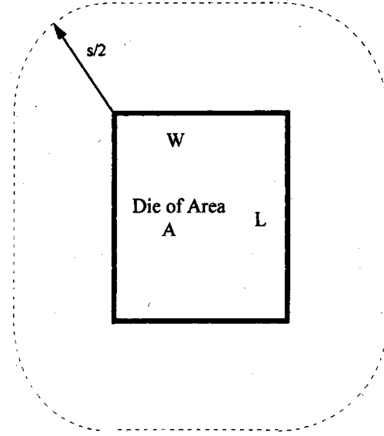


Fig. 2. Critical area sensitive to a defect of size s for a die of length L and width W.

The first term in (10), Y_d, is identical in form to that arising from the simple Poisson model as given by (1), with the yield depending exponentially on the product of the actual die area and the average defect density. If the defect size dependence of the critical area for point and small particulate defects is included in the derivation of (10), it is this term that will reflect such a dependence [9]. Note that in (10) the value of D_0 includes defects of all sizes, even those that are comparable to or larger than the die.

The second term, Y_s, is the yield loss term that results from the model only if there are larger-size defects. In such cases the exponent includes both a constant or die-area-independent term and a term dependent on the sum of the die length and width, the magnitudes of these two terms being functions of the defect size distribution. The die-area-independent yield loss contributor in (10) can be viewed as an analytical expression for that portion of the Y_0 in (3) and (4) that accounts for parametric yield loss. The additional large-defect yield term, which is effectively dependent on die perimeter, is interestingly a term that has been postulated in the past but without theoretical justification [13]. In his work Moore found that the yield could be approximated by assuming it varied exponentially with the square root of the die area, which, in the case of a square die, is proportional to the die perimeter. For interpretive purposes this term can be viewed as accounting for the added die lost around the edges of the larger parametric defects which only partially overlap as shown in Fig. 1. As a result, (6) and (10) provide a unified model which includes both small defects and large-area defects such as parametric yield loss mechanisms through a single distribution of defect sizes.

It should be noted that the yield analysis provided here is not restricted to only the parametric area yield losses described, but will also apply to any other large-size defects such as scratches and handling problems around the edges of wafers which are subject to the argument presented using Fig. 1. All such regions will result in a die-size-dependent yield loss caused by dice that only partially overlap the failure area. They will therefore be better approximated by an expression such as Y_s in (10) than by a multiplicative yield constant such as Y_0.

In the derivation of (10) the possible contribution of defect clustering effects as represented by (2) has not been included. However, it is straightforward, although perhaps complex, to develop yield expressions using (10) and (2) which incorporate any combination of defect clustering and variable defect sizes. No attempt will be made here to expand on the derivation in this way. Rather the simple Poisson form of the variable defect size model as given by (10) will be used for comparison both to existing models based on clustering and to experimental data. In this way the unique features of the variable defect size model can be illustrated and its characteristics relative to clustering models can be clearly identified.

While (6) or (10) can be used as is for interpretation of experimental yield data, a two-parameter model is often easier to use for analysis and comparisons provided such a model provides good agreement with the data. It has been found that by assuming a specific defect size distribution a two-parameter model can be derived from (10) which provides surprisingly good agreement with the experimental yield data to be discussed later as well as simplifying the discussion. The size distribution assumed is given by

$$D(s) = (D_0/s_0)\exp(-s/s_0) \tag{11}$$

where s_0 can be looked upon as an average defect size. Substituting (11) into (10)

$$\begin{aligned} Y = Y_d Y_s &= \exp\{-LWD_0\} \\ &\cdot \exp\{-D_0((L+W)s_0 + (\pi/2)s_0^2)\}. \end{aligned} \tag{12}$$

Equation (12) provides, like the defect clustering models excluding Y_0, an expression containing two parameters D_0 and s_0 that can be chosen for best fit to experimental data. However, its form is quite different and the expression is applicable to both point defect yield problems as well as to some combination of point defects, larger size defects, and parametric yield limiters. Fig. 3 illustrates the die area dependence of yield predicted by (12) for different values of s_0 and D_0 in the case of a square die. Note that as the value of s_0 increases, in addition to changes in the shape of the yield versus die area curve the yield intercept corresponding to zero die area becomes less than unity.

It should also be noted here that in the case of devices designed with redundancy for yield improvement such as many memory devices, the redundant elements will be unable to cope with the larger defects that encompass a significant portion of the die. As a result, if the variable defect size model applies, it follows that effectively only Y_d in (10) and (12) can be improved by the implementation of redundancy.

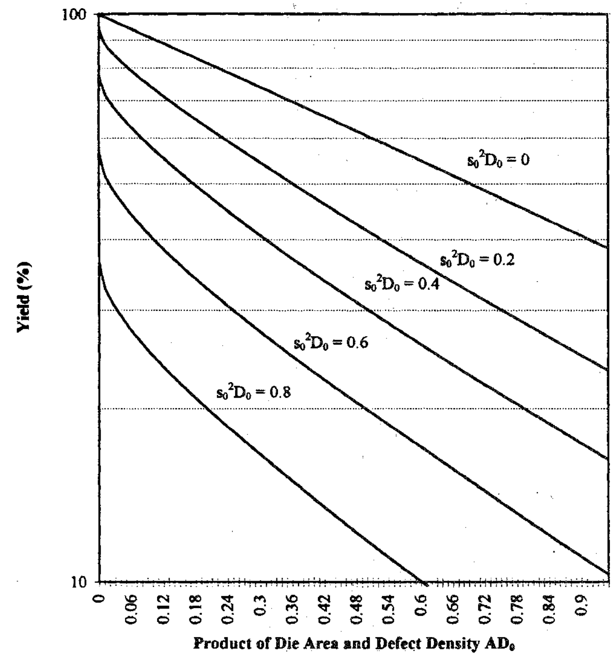


Fig. 3. Theoretical yield versus normalized die area for the variable defect size model.

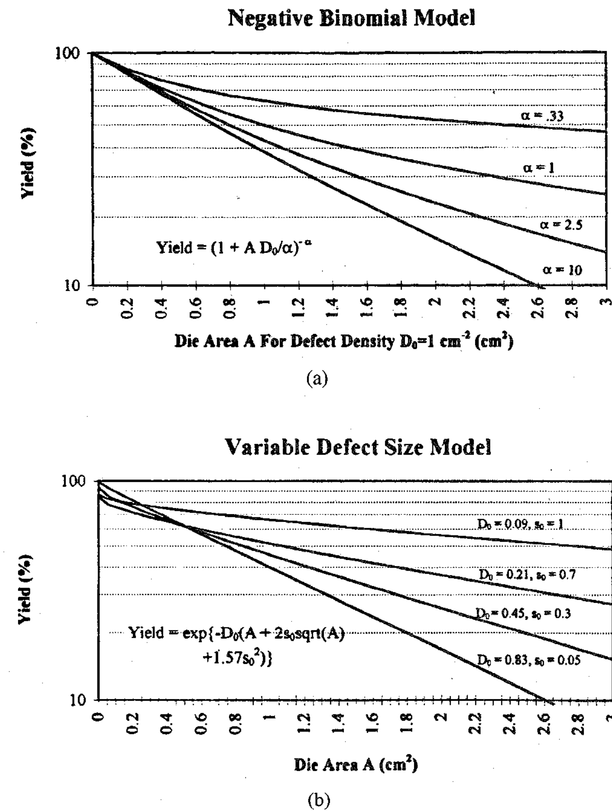


Fig. 4. Comparison of yield dependence on die area for the negative binomial model and the variable defect size model with parameters chosen to give similar curves.

III. Comparison to the Murphy Yield Model

While there are a number of assumed defect density distributions including those proposed originally by Murphy [1] that are used in practice, a number of authors [2], [3], [6], [7], [9], [14] have used the gamma distribution function, which results in the NB model given by (4), to explain experimental yield data. Since this distribution is representative of most of the features of clustering models in general, only a comparison to this model will be included here. Other assumed clustering

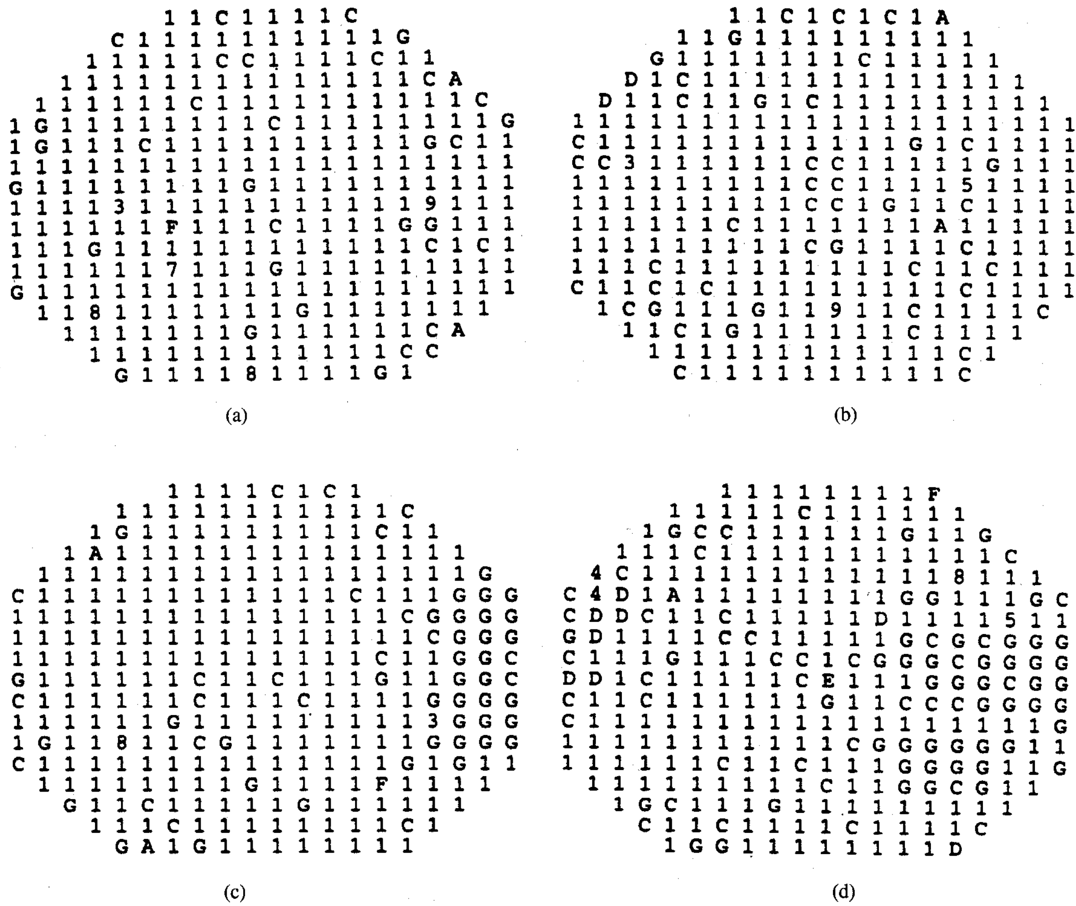


Fig. 5. Representative experimental wafer maps illustrating the characteristics of some large-area and parametric yield loss contributors.

distributions have been found to give similar results and conclusions.

Fig. 4 provides a comparison of the yield variation with die area predicted by this well-known NB model to the yield variation with die area predicted by the variable defect size (VDS) model given by (12) for a square die with parameters chosen to provide approximately similar curves. The value of Y_0 for the NB model has been assumed to be unity although the conclusions reached are valid for any value of Y_0. It can be seen that both models have similar shapes and die area dependencies except when the die area is small. Since most experimental data in the literature covers the larger die sizes, because of the similarity of the curves it can reasonably be concluded that if one model can successfully explain the observed and published die area dependencies of yield, then the other one can do so also. However, the explanation of the die area dependence of the yield clearly will be quite different for the two models. Thus, it can further be concluded that agreement with yield versus die area data alone does not provide complete evidence in support of either the VDS model or the various yield models based on clustering such as the NB model.

The quite different die area dependence of yield at small die sizes in Fig. 4 illustrates the fundamental difference between all defect cluster models and the VDS model presented here. In the case of defect cluster models, the yield for small die ($AD_0 < 1$) converges independent of the type or degree of clustering, and the yield dependence on die area must always become linear in the product AD_0 as the die area approaches zero. The implied assumption of the model is that the Poisson distribution is a good approximation for small die and that the often higher-than-expected yield of larger die (based on the defect density extracted from small-die data) is caused by defect clustering. By contrast the VDS model used here assumes no defect clustering and retains the assumption that a Poisson distribution applies for all defect sizes. However, it incorporates the fact that the die area dependence of yield for all die sizes is impacted additionally by a die-perimeter-dependent term.

IV. Comparison to Experiment

Parametric yield loss problems can often dominate over point-defect-related yield contributors, particularly during the early startup phase of new processes and on some performance-sensitive devices such as analog circuits and high-speed digital circuits. In addition to causing nonfunctional die, they may also result in yield losses such as the "good to functional" yield loss and bin-split yields where the die is functional but fails to meet specific performance specifications. However, even more mature processes or those with products

that exhibit rather low yield sensitivity to parametric variations often have some parametric yield loss.

Examination of yield wafer maps has shown that such parametric yield losses often cover only portions of wafers affecting a relatively small number of die, as discussed in the literature [11], [12]. Fig. 5 provides additional illustration of such characteristics. A number of representative experimentally-observed wafer maps for a logic device fabricated on the relatively mature production CMOS process used in this study are shown, where numbers or letters representing the test results are placed at the locations of the die on the wafer. The number 1 indicates good devices and the other numbers and letters represent various types of failure modes. Fig. 5(a) shows the map of a wafer which exhibits no obvious parametric or systematic types of failure, and the expected random distribution of both failed die and the nature of the failure mechanisms is observed. However, the other wafer maps shown in Fig. 5(b)–(d) illustrate types of yield loss features exhibited by some wafers. Not only are some of the failures spatially localized over some fraction of the wafer area within which the yield is zero, there is a commonality to the test that most die tend to fail in these regions. In Fig. 5(b) there appears to be a localized region near the center of the wafer where devices fail test "C"; in Fig. 5(c) and (d) there are larger regions on the right side of the wafer where devices fail test "G."

Such localized regions or areas of zero yield might be viewed as having very high densities of small defects, and interpreted in terms of defect clustering. However, if the devices are functional but simply fail performance tests, or in many cases when there is a commonality of the fail bin in the zero-yield regions as shown, this behavior is often indicative of parametric yield loss rather than loss due to small defect effects. Independent of their cause, however, an alternative interpretation to that of defect clustering is to treat these zero-yield regions as rather large random defects causing failed die if any portion of a die overlaps the region, as assumed in the variable defect size model presented here. The wafer maps shown tend to support such an interpretation. In particular they show that such yield loss regions often extend over several dice but are smaller than the wafer, and that the appearance of such regions as well as their size appears to be random as assumed in the VDS model.

In order to further illustrate the validity and applicability of the model, experimental yield data on one device from five lots of approximately 24 wafers each, run in the controlled production CMOS process described above at a 6″ wafer commercial semiconductor factory over a period of about a year, were analyzed. From wafer maps of good dice, it was possible not only to establish the yield of individual devices, but also to establish the yield of independent device pairs as well as that of independent groups of 3, 4, 6, 9, 12, and 16 [15]. In this way the data could be used to generate yield versus die area curves with the assurance that both $\langle s \rangle$ and $\langle s^2 \rangle$ in (6) and (10) must be the same for all cases. Fig. 6 shows the comparison of the experimental data to best-fit yield predictions using the two-parameter VDS model with the values of s_0 and D_0 given in Table I. Table I also provides

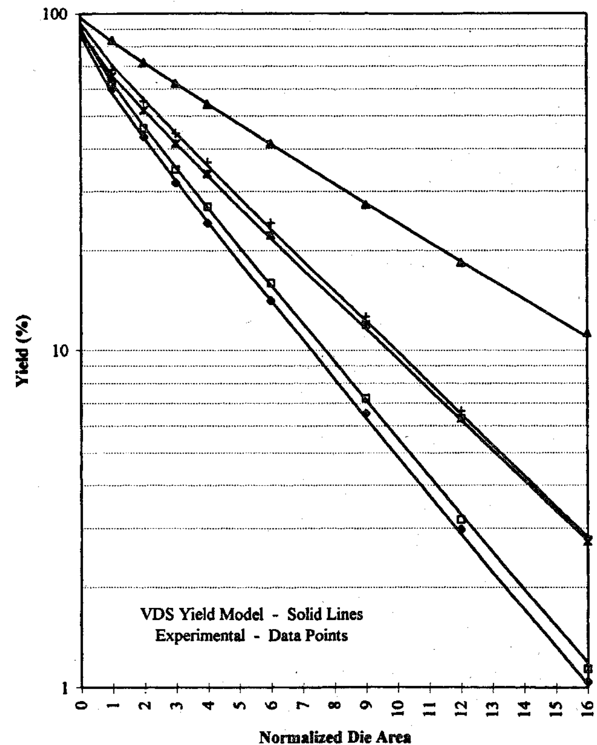


Fig. 6. Experimental yield data from five wafer lots, with best fit prediction based on the variable defect size yield model.

an indication of the magnitudes of the two yield terms, Y_d and Y_s relative to overall yield Y for these particular wafer lots. Fig. 7 shows a similar comparison of the experimental data to best-fit yield projections using the three-parameter NB model with the values of Y_0, D_0, and α given in Table I under the assumption that the critical area is equal to the actual die area. The three-parameter NB model was used rather than the two-parameter version not only because of the better fit to the data, but also because it includes parametric effects through the multiplicative term Y_0.

Figs. 6 and 7 illustrate that both the VDS and NB models provide excellent agreement with the experimental data given that appropriate parameters are chosen for the models. Thus it can be concluded that both models can adequately and independently account for the observed yield dependence on die area. As a result it is not possible to determine from this agreement alone that one or the other model is more representative, or whether some combination of the two models applies.

However, depending on which model one assumes, somewhat different conclusions will be reached with respect to the relative contribution of different yield loss mechanisms. From Table I it is seen that the VDS model tends to predict somewhat smaller defect densities and therefore a somewhat larger yield loss contribution from large defect and parametric effects than the NB model. Because of the different underlying assumptions in the two models, the fact that the VDS model predicts smaller defect densities is always expected to occur although the magnitude of the difference will vary depending

TABLE I
BEST-FIT THEORETICAL VALUES FOR YIELD PARAMETERS USED IN FIGS. 6 AND 7

	Wafer Lot 1	Wafer Lot 2	Wafer Lot 3	Wafer Lot 4	Wafer Lot 5
Measured Yield (%)	60	83	66	69	62
VDS Model					
D_0 (cm^{-2})	0.28	0.15	0.22	0.23	0.28
s_0 (cm)	0.43	0.21	0.42	0.27	0.37
Y_d (%)	80	89	84	83	79
Y_s (%)	75	94	79	83	78
NB Model					
D_0 (cm^{-2})	0.37	0.18	0.28	0.30	0.37
α	20	13	16	12	15
Y_0 (%)	81	96	82	88	84

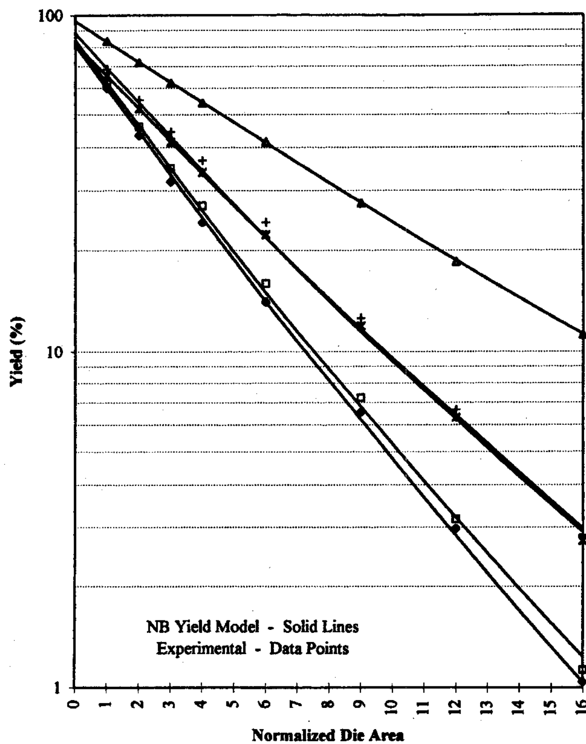


Fig. 7. Experimental yield data from the same five wafer lots, with best fit prediction based on the negative binomial yield model.

on the experimental data. In any case, any prioritization of yield causes which are based on the degree of fit to a yield versus die area plot will differ depending on which yield model is used. Therefore for accurate separation of the relative contribution of the small defects from that of the larger and parametric defects, it will be important to use the most representative yield model.

If the VDS model is, in fact, a good approximation to the yield loss mechanisms applicable to the experimental data, then Table I shows that for these particular wafer lots the conventional Y_d term does not account for most of the yield loss. Much of the yield loss results from the larger-size defects reflected in the Y_s term. Detailed examinations of wafer maps from the five lots of wafers tends to be consistent with this conclusion, although it was not possible to correlate precisely the values of s_0 in Table I to physical observations. On the other hand examination of wafer areas clearly free of larger size defects tended to be represented by defect densities very close to those shown for the VDS model in the table.

V. DISCUSSION AND CONCLUSIONS

From Fig. 6 it is apparent that the VDS yield model presented here, even in its two-parameter form, provides excellent fits to the experimental yield data provided. When this result is combined with the fact that parameters can be chosen so that the VDS model can always closely approximate the yield dependence on die area predicted by defect clustering models, it seems reasonable to further conclude that by selecting appropriate values for $D_0, \langle s \rangle$, and $\langle s^2 \rangle$ the VDS model will satisfactorily match most experimental data of yield versus die area that can also be matched by defect clustering models. Thus it provides an alternative and quite different physical explanation to account for observed departure of yield dependence on die area from that predicted by the simple exponential relationship $\exp(-AD_0)$.

While such good fits are encouraging, curve fitting alone will clearly not provide justification for any specific model. Thus for any particular case additional information is needed to assess which model, or what combination of the variable defect size and defect clustering models, applies. However, in those cases where the VDS model is found to be consistent with more detailed assessments such as observations of wafer

maps, there are significant advantages in application to yield analysis. Not only are the statistical distributions involved well understood and straightforward to assess in terms of sampling plans, the simple exponential form of the equations resulting from the model allows the simple addition of terms in the exponent to account for the contributions of individual process steps or sequences of steps. As has been described by Ferris-Prabhu [8], a yield model with this feature is highly desirable because of its utility in quantitative assessments of both the magnitude and the size distribution of defect densities at individual process steps. Furthermore the model inherently includes the consequences of parametric yield loss mechanisms, yield limiters usually included separately through an empirical yield multiplier in other published models, and illustrates how such problems can affect yield as a function of die size. This can be of particular value in assessing the relative contribution of large-area and parametric versus small-defect yield limiters over the life of a semiconductor process.

A major feature of the model is an additional yield term that is dependent on die perimeter. Previous work has usually assumed that the areas of the wafer impacted by parametric problems and other large-size defects such as scratches are independent of die size, while the model developed here also accounts for the additional wafer area lost due to die around the periphery of such large defects that only partially overlap the defect. In those cases where such larger defects are significant yield loss contributors, interpretations of the die size dependence of yield can lead to incorrect conclusions if they are treated simply as a die-size-independent yield multiplier.

It should be pointed out that in the model developed here the defect density for the larger defect sizes could be die design/test dependent. This could come about, for example, if one device on a given process were more sensitive to transistor electrical parameters than another. Thus the model can be used to explain experimentally observed "scatter" in die yield versus area plots when different devices are run on the same process [6] and therefore subject to the same densities and clustering characteristics of the smaller defects. Alternately, bin-split yield for products on a wafer, where it is known that all devices will be impacted by the same small and point defects but may be sensitive in different ways to parametric variations, can be analyzed using the VDS model simply by using different larger-size defect distributions for the different bins. These can then be correlated to different parametric sensitivities for in-depth yield analysis.

The VDS model is also easily applied to devices that incorporate redundancy for yield improvement, although a study of this aspect of the model has not yet been carried out. Since most of the larger size defects will not be repairable using redundancy, the model inherently incorporates separation of those yield limiters which can be repaired from those that cannot, and allows application of simple Poisson statistics to redundancy issues. Alternative yield modeling approaches usually introduce additional adjustable parameters in order to separate repairable die from nonrepairable die for comparison to experimental data and to explain the amount of yield improvement attained with redundancy [14].

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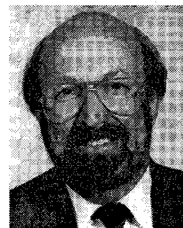

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