Figure 1  A three-stage distributed amplifier using CMOS n-FETs.

Figure 2  T-Section Network

Figure 3  Lossless cascade of T-sections forming artificial transmission line.
Figure 4 Lossy “gate” transmission line.

Figure 5 Lossy “drain” transmission line.
Figure 6a Gate line image impedance as a function of inductor cutoff frequency.

Figure 6b Gate line image impedance as a function of capacitor cutoff frequency.
Figure 6c  Drain line image impedance as a function of inductor cutoff frequency.

Figure 6d  Drain line image impedance as a function of capacitor cutoff frequency.
Figure 7a Gate line attenuation as a function of inductor cutoff frequency.

Figure 7b Gate line attenuation as a function of capacitor cutoff frequency.
Figure 8 Drain line attenuation as a function of inductor and capacitor cutoff frequency.
Figure 9 Bisected-\( \pi \) \( m \)-derived matching network.

Figure 10 Gate line input impedance using bisected-\( \pi \) \( m \)-derived matching network. Solid line shows performance for a lossless transmission line. Dashed curve shows performance with lossy matching network.
**Figure 11** Simple FET model used for analysis.

**Figure 12** Derivation of gate-voltage impedance as the $T$-section center impedance.
Figure 13  Gain as a function of frequency using Beyer’s ideal expression and the gain calculated in this work with and without an $m$-derived matching network in place.

Figure 14  Gain versus number of stages evaluated at low frequency (2 GHz).
Figure 15  Active load proposal to reduce gate or drain line losses.

Figure 16  Actively loaded gate attenuation constant in action. Propagatin constant remains imaginary (not shown).
Figure 17 Comparison between approximate and exact expressions for attenuation constant for low loss case (ideal passive devices).

Figure 18 Constant K-curves in $a$-$b$ plane.
Figure 19 Constant X curves in a-b plane.

Figure 20 Constant KX curves in a-b plane.
Figure 21  Gain-bandwidth curves in $a$-$b$ plane.

Figure 22  "Hand-calculated" 4-stage distributed amplifier design.
Figure 23  $S_{21}$ and $S_{11}$ of 4-stage design with $C_{gd}=0$.

Figure 24  $S_{21}$ and $S_{11}$ of 4-stage design with $C_{gd}=30$ fF.
Figure 25  Four-stage optimized design.

Figure 26a  Gain of optimized design (green) versus ideal (blue) and non-optimized (red).
Figure 26b  Input match $S_{11}$ and gain $S_{21}$ of optimized design.

Figure 27  Noise figure versus frequency for 4 and 6 stage designs optimized for noise and gain-bandwidth.
Figure 28 Simulated noise figure of four-stage amplifier.